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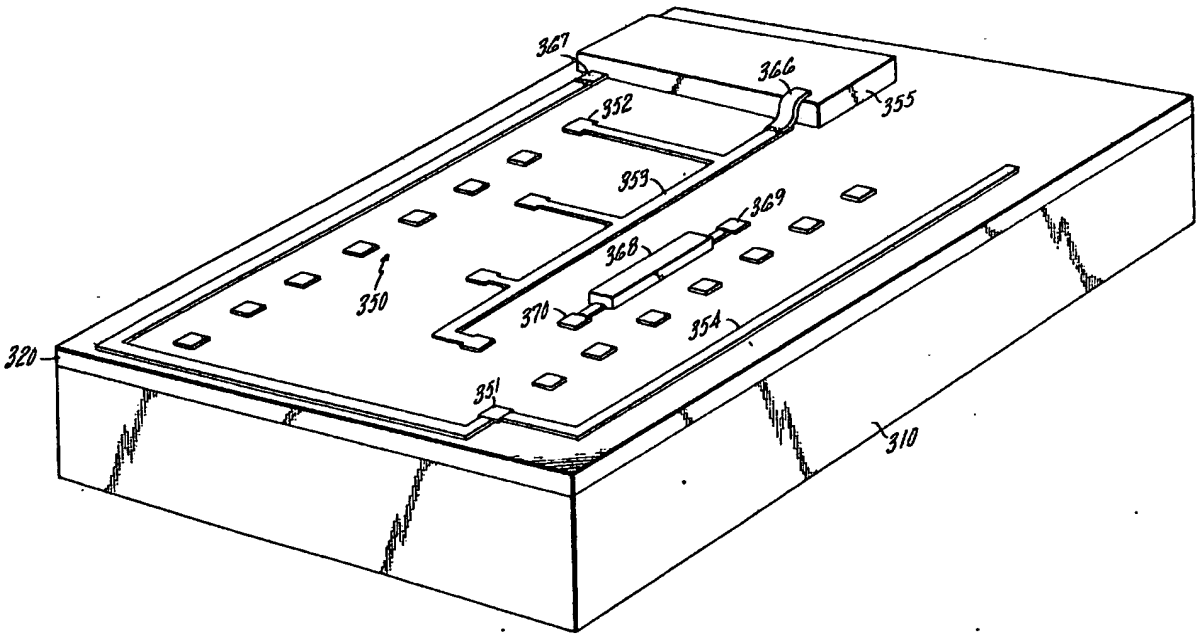

(57) Abstract

An integrated circuit device includes a conventional integrated circuit (310), modified by the addition of a dielectric layer (320) having a network of conductors (353, 354) on the top; together with one or more active or passive electrical components or devices (355, 368) connected between the top conductors.

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Description

Integrated Circuit Add-on Components

Technical Field

The field of the invention is that of a combination of an integrated circuit with another integrated circuit and/or with one or more components.

Background Art

It is known to provide two integrated circuits in the same dual in-line (DIP) package, as is done in the MK4332(D)-3 32K dynamic RAM from Mostek Corporation, Carrollton, Texas. In that case, two 16K RAMs employ the same support, being wire-bonded to a common set of leads, with the outputs of both 16K chips being tied together.

It is also known to combine one or more discrete components (such as an RC time constant circuit) to the pins of an integrated circuit socket.

It has long been known, however, that it is not practical with present technology to incorporate large values of resistance, capacitance or inductance within the semiconductor itself using conventional "front end" thin-film techniques.

Disclosure of Invention

The invention relates to a combination of an integrated circuit, having a contact surface that includes a number of contacts set in a relatively thick protective top layer, with one or more additional devices.

The additional devices may be discrete passive devices, such as resistors, capacitors, inductors, or connectors; simple active devices, such as power transistors or different technology transistors; or complex devices, such as a second integrated circuit or an optical device.

A feature of the invention is the combination of a MOS or CMOS first circuit with a bipolar second circuit, for use in applications, such as telecommunications, that require different voltage levels or higher power devices.

Another feature of the invention is the combination of a first standard integrated circuit with a second custom or semi-custom integrated circuit that has been developed for a particular customer or for a specialized application.

Another feature of the invention is the combination of an integrated circuit of one material, such as silicon, with a second device, such as a GaAs solid state laser, that uses a different semiconductor material from that of the first circuit.

Brief Description of Drawings

Figure 1 illustrates the process flow in a system using the subject invention.

Figure 2 illustrates the steps in Figure 1 in more detail.

Figures 3A and 3B illustrate integrated circuit chips used in the system of Figure 1.

Figures 4A and 4B illustrate alternative embodiments of the invention.

Figure 5 illustrates a portion of a leadframe.

Figure 6 illustrates a cross section of an integrated circuit suited to the application of the invention.

Figure 7 illustrates a method of attaching leads to an integrated circuit suited to the application of the invention.

Best Mode for Carrying Out the Invention

The present invention was developed together with the components of a system for assembling and testing integrated circuits. Other features of the system are the subject of co-pending patent applications, filed the same day herewith and assigned to the assignee hereof. In order to convey the invention in context, discussion of the overall system is included in this specification.

An overall flow chart of the steps used in the back-end assembly is illustrated in Figure 1, in which a number of steps are illustrated schematically and are performed by a variety of different machines in communication with and sometimes controlled by a computer for storing test and other data.

In the first major step, represented by the box labelled I, a process that may be part of the "front-end" or the "back-end", accepts as input a wafer that has been completed with all the conventional steps (including passivation - etc.) and applies a further layer of dielectric having a thickness sufficient to protect the chip circuits and to insulate them electrically from signals being carried on the top surface of the dielectric.

A pattern of metal leads is formed that extends from the contact pads on the previous chip to a

standard array of contact pads on the top of the dielectric. The standard array is the same for all chips having the same number of pins, regardless of the size of the chip die.

The wafer is then probe tested, in major step II with the results of the probe test being stored electrically, such as in a computer. The conventional ink-dot marking system for bad chips is not used.

The wafer is then adhesively mounted on an adhesive film in a frame holder that is shaped to allow for automatic insertion and orientation in various fixtures further along in the process and cut apart in an automatic sawing process (Step III) that cuts through the entire thickness of the wafer.

The good dice are then removed from the wafer in an automatic sequence (Step IV) that presses from above against the tape to selectively pick a die down into a dedicated carrier where it rests circuit side down. This is not a problem since the active circuitry is protected by the standard pad dielectric and standard pads. The wafer and punch-out device are moved under computer control to put the dice into the correct positions in the carrier.

The dice are transferred to a mating carrier simultaneously in an inversion operation that rotates the two-carrier "sandwich" by 180 degrees, so that the dice resting in the second carrier have contacts on the top side. A set of dice are transferred to a bonding fixture that holds a convenient number, illustratively 14 dice. Once loading is complete, a leadframe matching the spacing of the dice in the fixture is positioned above the dice in the soldering

fixture and an upper bonding fixture is added to maintain lead to pad contact during the bonding process.

The bonding fixture is heated to reflow the solder and form the interconnection (Step V).

The leadframe with dice attached is placed in a transfer or injection molding machine that encapsulates the die together with the interconnections to the leadframe (Step VI).

The molded strip of devices is then trimmed and formed conventionally (Step VII).

There is a representation in Figure 1 of data communication between the machines that perform the steps listed above and the controlling computer. Most data communication steps are optional. The step may indeed be performed under operator control and data may be written down manually. The benefits of automatic recording of data and error-free recall of data from a previous step will be evident to those skilled in the art.

Figure 2 sets out the steps in Figure 1 in more detail and also illustrates the material and data flow. A convention used in this figure is that a broken line indicates a material transport step of the sort of loading the material into a container and moving the container to another location and a double arrow indicates data flow into or out of a computer or other storage device. The three material inputs to the process are the wafers, leadframes and plastic for encapsulation. Two recirculation loops involve, respectively, a frame used to support the wafers during the sawing and die selection steps and a positioning fixture used to maintain a set of dice in alignment with a leadframe segment during the bonding operation.

The different steps of the invention are set forth in more detail below and in copending patent applications filed on the same date herewith and assigned to the assignee hereof.

Standard Contact Pads

Returning to the first major step, the illustrative dielectric layer is a polyimide such as Dupont 2525 applied with the thickness of 6 microns and cured at a temperature of greater than 260 C. There may be a nitride or other layer below the polyimide to improve adhesion to the reflow glass or other top layer. The electrical contact pads that have been previously formed in the integrated circuit chip by conventional processing techniques are exposed by applying a photoresist, either liquid or in the form of a tape, on top of the dielectric and etching down through it a passageway to the metal contact pad in the circuit in a conventional manner. A "via" will be formed by filling the contact holes with a metal or other conductor until the surface of the dielectric is reached. The photoresist is stripped off and a layer of metal is applied by any technique, such as sputtering, over the surface of the polyimide. In one example, the polyimide was back sputtered to prepare the surface, after which 600 Angstroms of 10% titanium +90% tungsten followed by 3 microns of copper were sputtered on. A second layer of photoresist is applied and patterned to define a set of metal leads in the metal layer. The leads reach from the vias penetrating the dielectric to an area in the center of the chip which has a standard pad array of pad contacts that may advantageously be

the same for two or more chips that have the same number of leads. For example, a 16 pin chip will have the same standard pad array, of size about .016" by .016" in a standard configuration having dimensions of .126" by .126", whether it is a memory or any other logic device. The standard pad array will be sized so that it fits on the smallest chip that is to be used with that leadframe.

The exposed areas of the metal are plated with a solder composed of a standard mixture of lead and tin in a conventional electrolytic plating process that employs a mixture of 95% tin and 5% lead. The photoresist is stripped and the plated areas of the metal layer are used as an etching mask in the next step in which the remaining unwanted area of the metal layer is etched away in a bath of hydrogen peroxide plus ammonium hydroxide followed by hydrogen peroxide, which does not attack the solder.

There now remains a chip 300 of the form illustrated in Figure 3A, in which die 310 has on it a thick layer of polyimide 320 and a network of metal lines 326 leading from the contact areas 330 on the outside of the chip to the standard pad array 340. The metal lines 326 have lower inductance, greater thermal conductivity and greater strength compared to the wires that were previously used. Lines 326 are the second set of conductors in the die, the first set being the metallization and/or polysilicon conductors below the dielectric layer.

In the example shown in Figure 3A, the first contacts and the vias through the polyimide layer are all formed on the perimeter of the chip. This figure illustrates a chip in which the layout design was

made for the old wire-bonding method in which the contact areas had to be on the perimeter of the chip. An advantage of retaining the old design, besides saving the expense of a new layout, is that it is possible to use conventional wirebonding processes when added capacity is required. To do this however, requires that the additional dielectric and metallizations for the standard pad process is not used.

It is also possible to use the invention and put the contact areas through the dielectric at any convenient location, as shown in Figure 3B. The vias for these leads are shown as originating at different locations on the chip surface, not exclusively at the edge as was the case in the prior art. Lead 348 is shown as connecting a via that is located within the standard pad array. Lead 343 is connected to a via-section 344 through a bridge, not shown in the drawing, that is placed on top of the passivation layer of the underlying chip below the polyimide. This illustrates an additional degree of freedom in routing leads and placing components that is provided by the invention.

A via 305 is shown in Figure 3A in a cut-away portion of the figure as extending from a lower contact area 304 to an upper contact 306 at an end of one of leads 326. The lower contact pads in current practice are typically 4 mils by 4 mils. With such a large area to make contact, the alignment tolerance for the formation and location of the vias and the placement of leads 326 are typically $\pm$ 2 mils to 3 mils, which is much greater than a typical tolerance of $\pm$ 1/2 mil to 1 mil for connecting leads in the precision processes that are used with conventional wirebonding.

The steps of forming vias and putting down leads may be performed in the front-end using the standard machines for photolithography, if that is convenient. Since the requirements for putting down these metal leads are much less stringent in position alignment than the usual front-end work, it may be preferable to use thick-film technology, such as screen printing, to pattern the dielectric and top leads. Typically, the thick-film technique will be 1/4 to 1/2 the cost of the precision techniques.

It has been found that the polyimide layer 320 of Figure 3 does not adhere reliably if it is attached directly to the layer of oxide immediately below it. A cross section of a portion of a die is shown in Figure 6, in which substrate 6-100 is the silicon substrate and aperture 6-200 is the "street" that separates adjacent dice. The width of a street is typically 100 microns, to allow room for the saw kerf in the separation step that is performed with a diamond saw having a width of .001 inch.

A contact pad, 6-05, is shown with a series of apertures defined above it. Pad 6-05, which is typically aluminum and is connected by metallization strips, not shown, to the rest of the circuit, is surrounded by oxide 6-10, which has a conventional composition of SiO_2 plus phosphorous and other additives and a thickness of 1 micron. Oxide 6-10 has a top surface 6-15 on which polyimide layer 6-50 was, at first, applied directly. Early tests showed significant difficulty, in that polyimide layer 6-50 (layer 320 in Figure 3) often disbonded, causing the leadframe to pull the polyimide away from the underlying layer.

Oxide 6-10 functions as the top dielectric layer in the circuit. It not only coats the substrate and contacts, as shown in Figure 6, but also the circuit elements and metallization.

Passivation of the active elements of the circuit is effected in the usual manner of silicon MOSFETS by the thin oxide over source, drain and active area so that oxide 6-10 functions purely as a dielectric, not as a passivating layer.

Nitride layer 6-20 is deposited by plasma-assisted CVD at a temperature of 250 C, in a conventional manner, to a thickness of .3 micron after street 6-200 has been etched through oxide 6-10 to the substrate. A layer of 2525 polyimide from Dupont is applied and spun to produce a relatively flat top surface. Apertures 6-45 above contact 6-05 and 6-55 above street 6-200 are opened through the uncured polyimide by wet etching with a conventional basic solution such as Shipley 312 developer. Typical dimensions for the top of aperture 6-55 and 6-45 are 100 and 87 microns, respectively. After aperture 6-45 has been opened, aperture 6-40 is opened through nitride layer 6-20 in CF4. A typical dimension of aperture 6-40 is 75 microns, so that aperture 6-40 is surrounded by nitride 6-20 and does not expose any of oxide 6-10.

It has been found that the adhesion of polyimide to top surface 6-25 of nitride 6-20 is greatly improved over the adhesion of polymide to oxide 6-10 at surface 6-15. Nitride 6-20 adheres well to oxide at surface 6-15. the function of nitride 6-20 is thus to improve the adhesion of the polymide by means of a structure that totally encloses the oxide 6-10, not only at the vias but also at the saw cuts on the streets.

Probe Test

The next major step II is a test with the individual circuit dice still remaining in the wafer. A conventional wafer electrical test step could be performed in which small probes are attached to the contacts that will be used for the input/output and the individual chips are tested. An advantage of this invention is that the metal leads on top of the polyimide cover a much larger area than the old-style contact pads do, so that it is easier to make electrical contact at reduced pressure of the electrical contact probe or electrode with these large metal pads than it is with the small contact pads used in conventional techniques. It is also possible to make electrical contact to the leads before you reach the contact area, thus providing additional flexibility in the probe step. An important economic benefit from the invention is that only a single set of probe tips will be needed to match the standard pad array for the whole family of circuits that have the same number of pins. In the prior art, a different set of probe tips was typically needed for each chip design.

If the chip has optional electric contact pads outside the standard pad array, as shown by contact 350 in Figure 3B (which is a via formed to provide access to a point in a circuit that is to be tested, yet does not connect to one of the regular contacts), then a different set of probe pins will be needed in that case, of course.

In conventional wafer tests, defective chips are marked by a small dot of ink so that, in manual

assembly, they can be identified and discarded. In this process, the chips are identified electrically - i.e. the wafer is oriented in a particular way and the chips are identified by their locations in an X-Y matrix. The test data for individual chips are stored in the central computer memory or in a floppy disk or other storage medium and defective chips are identified in the computer. This step is referred to in Figure 2 as wafer mapping.

If the chip has the feature of redundant or optional circuits that are connected or disconnected by blowing fuses by a laser (as is done in large scale memory arrays), then this step will have been done before the polyimide layer is put down, as is currently being done. It is possible, however, to provide for the enabling or disabling of optional subcircuits or the enabling of redundant circuits to be done electrically by means of access through additional contacts (similar to contact 350) that are placed through the polyimide layer outside of the metal strips, or by putting down the polyimide with a large opening over the redundant circuits that will be closed later. In that case, the central computer would identify optional circuits that are to be enabled or disabled and blow fuses appropriately through the test probes. The point in the sequence at which fuse-blowing is to be done is optional, of course.

If the wafers have not been given an identifying label before, it is now necessary to put a label on them in order to maintain the connection between the test data stored in the computer and the wafer the data came from. There are many ways of doing this

correlation, of course, and no particular method is required. One preferred method is to put the identification on an identifying label, such as an optical bar code, that identifies the wafer. Another method is to form a programmable memory in the wafer in which the identities of defective chips may be stored. In that case, the wafer carries with it the necessary information so that there is no problem of getting the wafer separted from the test results.

Bond

The assembly for the final bonding step (Step V in Figure 1 and Leadframe Fixture Assemble, Bond, Disassemble in Figure 2) is shown in an exploded view in Figure 7, in which holder 7-110, represented schematically, holds 14 chips with the correct spacing, only two of the receptacles 7-225 being shown. Above receptacle 7-225, there is positioned chip 7-230 and, above the chip, a set of finger contacts 5-122 in leadframe 5-100, part of leadframe strip 5-125. The details of the leadframe will be described below. Cover 7-120 presses down on edge 5-110 of leadframe strip 5-125, which edges rest on shelves 7-112 to position the outer parts of the strip so that the contact tips will be deflected slightly. This deflection is done to compensate for inevitable fluctuations in the position of the tips during the manufacturing process, so that reliable contact is ensured during the bonding operation. The deflection is effected by making the depth of receptacle 7-225 such that the top of chip 7-230 projects above the plane of shelves 7-112 by a set amount. The amount of deflection, (.005 inch to .007

inch) is illustratively several standard deviations of the nominal fluctuation of the tip position to ensure reliable joint formation. The edges 5-110 of leadframe strip 5-125 will be forced on to shelves 7-112 by cover 7-120 and tips 5-122 will thus be pressed against the pads by the spring constant of the leads.

A typical leadframe used in the invention is illustrated in Figure 5, in which half of an individual frame is shown. The individual leadframes are stamped out of a ribbon of metal that may be an inexpensive copper alloy, in contrast to the expensive alloy having the correct thermal properties that is used in the standard prior art process. Strips 5-110 on either side of the ribbon serve to carry the actual leads 5-120 along. Leads 5-120 have an exterior end 5-123, shaped either for insertion in a socket or for surface-mounting, and an interior portion 5-121 for attachment to a die. The two portions are joined by segments 5-124 that will be severed after the bonding step. Holes 5-112 are provided to give a reference in positioning the leadframe. At the end of each lead segment 5-121, there is a region, 5-122, in which the lead is bent in a quarter circle (or bent twice to form a parallel contact section) to form a standard dimension flat contact area. Each of the different lead segments 5-121, with its different length, has been shaped to provide substantially the same spring constant so that the contact areas 5-122 will be uniformly pressed against the mating pads on the die to give correct alignment for the soldering operation. The leads 5-120 have been tinned with solder in a previous step in the fabrication of the lead frame ribbon.

It is an advantageous feature of the system, but not an essential one, that a family of chips that have the same number of pins have the same standard pad array on top of the dielectric. For illustration, two dice 5-130 and 5-132 of different size are shown together with the leadframe. With this feature, it will then be necessary to have only one ribbon of leadframes for the entire family of chips, with substantial savings in inventory.

Both the contact pads 342 of the die and the tips 5-122 have been tinned and are ready to be heated. The bonding is done by a vapor phase reflow soldering technique or other means of heating the materials to reflow the fusible alloys. These alternative techniques include infra-red heating, conveyor ovens, hot gas heating or laser heating. In vapor phase reflow, a liquid such as Flourinert FC-71 is maintained at its boiling point, the liquid having been selected so that its boiling point is above the soldering temperature. The soldering assembly of holders 7-110 and 7-120, with chips plus leadframe maintained in alignment, is inserted into a container or oven that is filled with the vapor at the boiling-point temperature and held there until the solder has melted and flowed to form a bond. A typical length of time for the heating cycle is 5 to 15 seconds. This boiling point temperature is typically above 225 degrees C but below 300 degrees C. In contrast, the present wire bonding and die attach steps are performed at temperatures of up to 460 degrees C and performed individually. In order to reduce the length of the heating cycle, the bonding fixture should have low mass and many

apertures to permit the vapor to flow freely about the solder joints. Holders 7-110 and 7-120 have been shown schematically in order to reduce the complexity of the drawing.

An important economic benefit of this invention is that all the leads are soldered at the same time. This is in contrast to the wire-bonding technique, in which the leads must be bonded one by one. The soldering step takes no longer for a 28 pin chip than it does for a 16 pin chip.

Mold

In the next major step, (Step VII in Figure 1), leadframe 5-100, with 14 chips attached, is placed into a transfer or injection molding machine to mold plastic about it, thus encapsulating and protecting the chip in a dielectric shell. The molding process will be done using conventional techniques and equipment. Any other method of protecting the chips may be used, such as ceramic holders. It is an advantageous feature of this invention that the wide contact area between the leadframe and the contact pads is extremely rugged compared to the wire bonding technique that is in standard use so that a far smaller fraction of chips will be damaged during handling and the chips can be moved about at a greater rate and with less delicacy required. It is a further advantage that the leads conduct heat away from the chip during operation.

After the encapsulated dice, (still in the leadframe) are removed from the molding machine, the optional labelling step of Figure 2 is performed. The dice identity first appeared during probe test,

when data were measured that applied to an individual die. That identity was preserved by the labels on the wafer, tape frame and leadframe, the computer being updated as required to log the die identity on the leadframe. Each chip may be marked by a laser branding process or any other convenient technique with an identifying label, test results, etc.

The conventional "dejunk" step, in which excess plastic is removed from the leads is also performed at this time.

Trim/Form

Next, in step VIII of Figure 1, the chip plus leadframe combination is separated from the ribbon and the spacing segments 5-124 that served to maintain the leads in correct alignment are severed. If the ribbon is formed from a sheet of copper or copper alloy, it is necessary to sever the connections 5-124 or else all the leads will be shorted together. If another version of the ribbon is used, in which a plastic backing is used for the portion 5-110 and to support leads 5-120, on top of which a plated copper lead has been formed, then it will be easy to maintain the sections 5-124 in plastic and it is not necessary to separate the leads.

It should be noted that the application of the present invention does not depend on the complete system described above; and the invention is not limited to the system described above. Those skilled in the art will readily be able to apply the present invention to many types of assembly and packaging systems. The application of the present invention to illustrative embodiments is described in detail below.

Discrete Component Attachment

The standard pad array of Figures 3A and 3B used a square outline that was sized to fit on a very small chip, so that a single leadframe could be used for the complete size range. There may be other technical or economic considerations, however, that justify a different pad array (which may still be common to a number of integrated circuits).

In one embodiment of the invention, Figure 4A shows a die having the same substrate 310 and polyimide 320 as before, but in which the pad array comprises two rows 350 illustratively of eight pads each, set toward the outside of the chip. With the center clear, there is room for bus 353, which distributes the power supply voltage to various points in the circuit, one of which is a via indicated by the numeral 352 and positioned at one of the array positions to make contact with a lead. Compared with the prior art technique of using thin wires, bus 353 offers considerably less resistance and inductance. Similarly, bus 354 makes contact with pad 351 and distributes the ground terminal about the die.

A further advantage of the sturdy polyimide layer 320 is that discrete electrical devices, active or passive, may be placed on top of layer 320 and connected to the circuit, either by vias or to the standard pads. In Figure 4A, device 368 is shown as being connected to vias 370 and 369. The device may be a thick-film resistor having a large magnitude (that is difficult to achieve with conventional integrated circuit techniques). Thick-film

resistors, capacitors and inductors are conventionally formed by silk-screen techniques on printed circuit boards. The capacitors require a three-layer "sandwich" of two conductors and an insulator.. The vehicle for carrying the conductor may be a conductive ink, epoxy or polymerizable material, or any other conventional technique. It also may be a separately formed device, optionally with conventional surface-mounted-device packaging and leads. Examples are resistors, inductors and capacitors. For purposes of this application, the term "top electrical device" will mean any thing from a conductor to an integrated circuit that is placed on top of layer 320.

One useful example of a capacitor is shown as unit 355, a charge reserve capacitor connected between the power supply and ground using a conductive adhesive at point 367 and to strap 366. Such capacitors are conventionally attached to integrated-circuit sockets to maintain a stable supply voltage when circuits switch. The economic advantages of including the capacitor with the chip are evident. A device such as unit 355 may be connected to any point in the circuit, of course.

One variation that is of great interest is the use of a separate device 355 that is an optical or other element that is difficult to fabricate on the same substrate. For example, device 355 could be a solid-state laser using a gallium arsenide substrate and die 310 could be a conventional silicon integrated circuit. In that case, a fiber-optic pigtail would be included for communication to other optical devices.

Other devices that may be readily implemented are an R-C timing network, either fixed or having an adjustable element for which an access hole is formed in the encapsulating plastic; or a power transistor using the area of device 355 to spread the heat load. Heat sinks may also be attached directly to layer 320 or to vias that provide a low impedance thermal conduction path from high-power sections of substrate 310.

These other devices may be attached in any convenient manner. They may be adhesively attached before or after the soldering of the leadframe (or they may be soldered and the leadframe adhesively attached). Alternatively, soldering or gluing of leadframe and discrete devices may be done simultaneously, with the leadframe maintained in position prior to bonding by an adhesive.

Figure 4B illustrates another variation of the invention that offers considerable reduction in inventory. There is now a two-chip assembly comprising a first chip 300' having substrate 310, polyimide 320 and surface pads as before, and a second chip 380 comprising substrate 310', polyimide 320' and array of contacts 382' that mate with an array of contacts 382 on layer 320.

An alternate U-shaped contact array 350' is shown, which has the advantage of freeing up half of layer 320 for chip 380. In order to bring all the leads over to one half of chip 300', it may be necessary to permit some variation in the spring constant of the leads.

Only some connections between contacts 350' and 382 are shown, for power supply and ground. Chip 380

may connect directly to the leads for input/output, of course. In the case illustrated, chip 380 is a ROM that needs only power supply and ground and communicates only with the larger chip through vias in array 382 or through surface leads, such as lead 373.

One particular application of great commercial interest is that of a multi-purpose chip, such as a single-chip microcomputer that is customized by adding a ROM. If the ROM is a mask option, then there must be a reserve supply of customized microcomputers to allow for fluctuations in the yield, or rush orders and the manufacturer must maintain an inventory of chips that are good only for one customer. With the embodiment of Figure 3D, however, the inventory for each customer need only be his ROMs, which are much cheaper than microcomputers. The manufacturer will maintain a reserve of microcomputer chips sufficient to meet the needs of all his customers, of course. It is evident that the total value of inventory will be less with a central reserve, simply because of the laws of statistics.

A variation of the two-chip system is that in which the main chip 302 is a generalized system, such as an input controller and the second chip 380 is one of a number of alternatives, each customized for a particular application. For example, the main chip might be a 5-volt logic chip and chip 380 might be designed to withstand the high voltages of the telephone network in a telephone interface such as a modem or coder.

Many other applications of the second chip, such as interfaces to different manufacturers' computers

for plug-compatible systems; or the implementation of one of a number of standard logical functions, such as a parallel output or a serial output, will be evident to those skilled in the art.

One convenient method of attaching chip 380 is to form pads 382' with a sufficient amount of high temperature solder to make reliable contact and to reflow that bond before bonding the leads at a lower temperature. Another method is to adhesively attach chip 380 in alignment and to solder both sets of contacts simultaneously.

Those skilled in the art will readily be able to apply the invention to many other embodiments; and the scope of the claims is not meant to be restricted to the embodiments shown. In particular, it is not necessary to the practice of the invention in its most general form that a leadframe be soldered simultaneously to all the contracts, and the invention may be applied with serial attachment of leads.

Claims

1. An integrated circuit device comprising:

a semiconductor substrate having an integrated circuit formed thereon;

a first network of electrical conductors for interconnecting selected components of said integrated circuit;

a plurality of exterior electrical leads connected to said circuit; and

an enclosing dielectric shell for enclosing at least said substrate and integrated circuit, said electrical leads passing through said shell for connection to other electrical devices;

characterized in that said shell further encloses a dielectric top layer having a second network of electrical connectors disposed thereon, said second network of electrical connectors being connected to said first network of electrical connectors through a plurality of vias in apertures through said dielectric top layer; and

said shell further encloses at least one top electrical device connected to said second network of electrical connectors.

2. An integrated circuit device according to claim 1, in which said at least one electrical device includes a bus bar connecting at least two of said vias to at least one of said exterior leads.

3. An integrated circuit device according to claim 1, in which said at least one top electrical device includes a passive electrical component connected between two points in said second network of electrical conductors.

4. An integrated circuit device according to claim 1, in which said at least one top electrical device includes at least one active electrical device.

5. An integrated circuit device according to claim 1, in which said at least one top electrical device includes at least one optical device.

6. An integrated circuit device according to claim 1, in which said at least one top electrical device includes at least one integrated circuit.

7. An integrated circuit according to claim 3, in which said at least one top electrical device includes a thick-film passive device.

8. A method of fabricating an integrated circuit device comprising the steps of:

a) forming an integrated circuit in a semiconductor substrate by a thin-film technique;

b) forming a first network of electrical conductors for interconnecting selected components of said integrated circuit;

c) placing a dielectric top layer above said first network;

d) forming apertures above selected points in said first network;

e) forming a second network of electrical connectors on a top surface of said top layer of dielectric, connecting said first and second networks through said apertures; and

f) connecting at least one top electrical device to said second network.

9. A method according to claim 8, in which said step of forming apertures comprises the steps of applying a sheet of photosensitive material above said dielectric, patterning said photosensitive material with aperture regions, and chemically removing that portion of said dielectric below said aperture regions to form said apertures.

10. A method according to claim 8, in which said step of forming said second network of electrical connectors comprises the step of applying a thick-film pattern of conductive material to form said second network.

11. A method according to claim 8, in which said step of connecting said at least one top electrical device includes the step of applying a thick-film pattern of electrically resistive material between two points in said second network to form a thick-film resistor from said thick-film resistive material.

12. A method according to claim 8, in which said step of connecting said at least one electrical device includes the step of forming a thick-film capacitor connected between two points in said second network.

13. A method according to claim 8, in which said step of connecting said at least one electrical device includes the step of forming a thick-film inductor connected between two points in said second network.

[received by the International Bureau on 15 July 1985 (15.07.85);
original claims 1-7 and 10-13 cancelled; new claims 3-5 added; claims
8 and 9 amended (2 pages)]

3. A method according to Claim 1, in which said step of connecting said at least one top electrical device comprises electrically and mechanically connecting a pre-formed active electrical device to said second network.

4. A method according to Claim 3, that further includes the steps of forming a first array of electrical contacts within said second network; mechanically attaching a second integrated circuit device having a second matching array of electrical contacts to said integrated circuit device with said first and second arrays of contacts electrically touching; and

making electrical contact between said first and second arrays of electrical contacts.

5. A method according to Claim 4, in which said step of forming an integrated circuit includes the steps of forming an undifferentiated integrated circuit and which further includes the steps of forming by thin-film techniques a specialized integrated circuit adapted to customize said undifferentiated circuit to a particular application; and in which said step of attaching said second integrated circuit device includes the step of attaching at least said specialized integrated circuit.

--Claim 8 (Amended) A method of fabricating an integrated circuit device comprising the steps of:

a) forming an integrated circuit in a semiconductor substrate by a thin-film technique;

b) forming a first network of electrical conductors for interconnecting selected components of said integrated circuit;

c) placing a dielectric top layer above said first network;

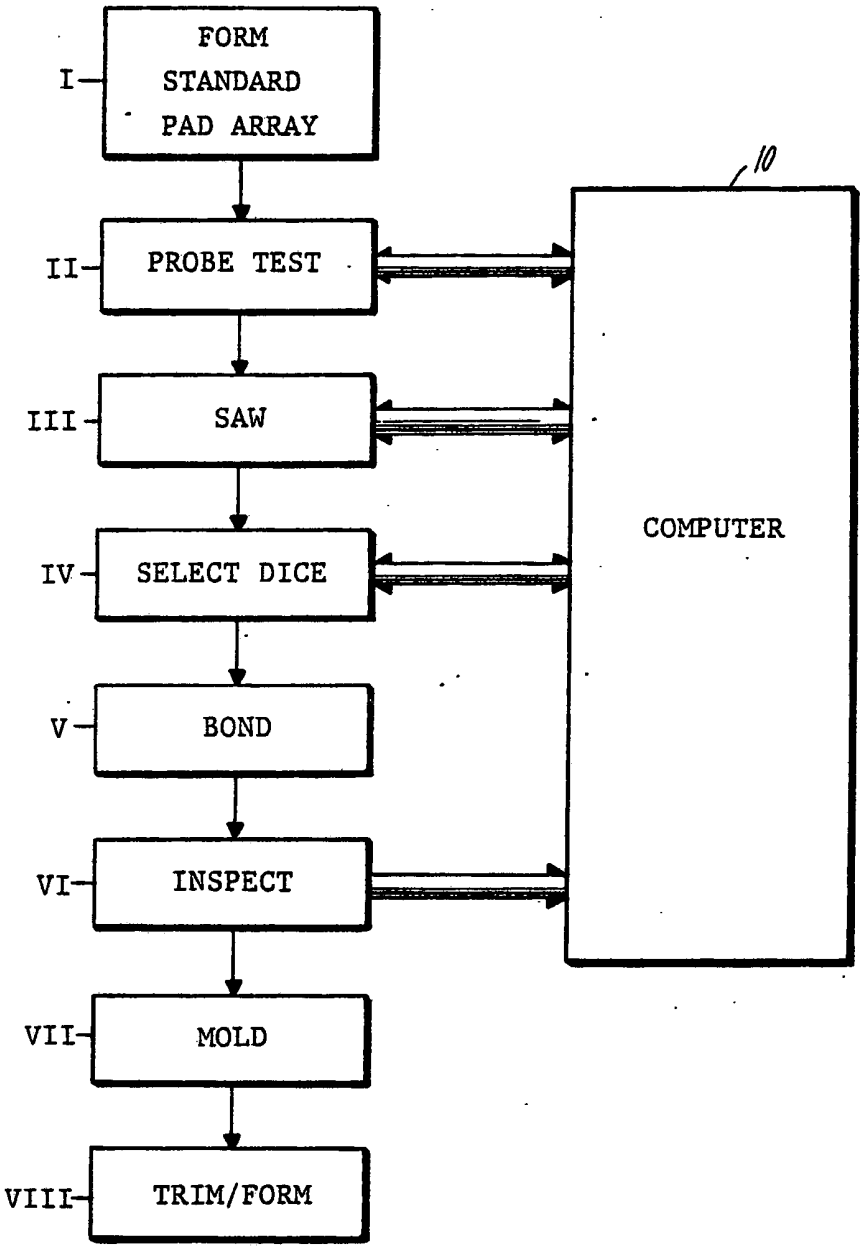
d) forming apertures above selected points in said first network;

e) forming a second network of electrical connectors on a top surface of said top layer of dielectric by applying a thick-film pattern of conductive material connecting said first and second networks through said apertures; and

f) connecting at least one top electrical device to said second network.--

9. A method according to claim 1, in which said step of forming apertures comprises the steps of applying a sheet of photosensitive material above said dielectric, patterning said photosensitive material with aperture regions, and chemically removing that portion of said dielectric below said aperture regions to form said apertures.

FIG. 1


I
FORM STANDARD PAD ARRAY
10
II
PROBE TEST
III
SAW
IV
SELECT DICE
V
BOND
VI
INSPECT
VII
MOLD
VIII
TRIM/FORM
COMPUTER

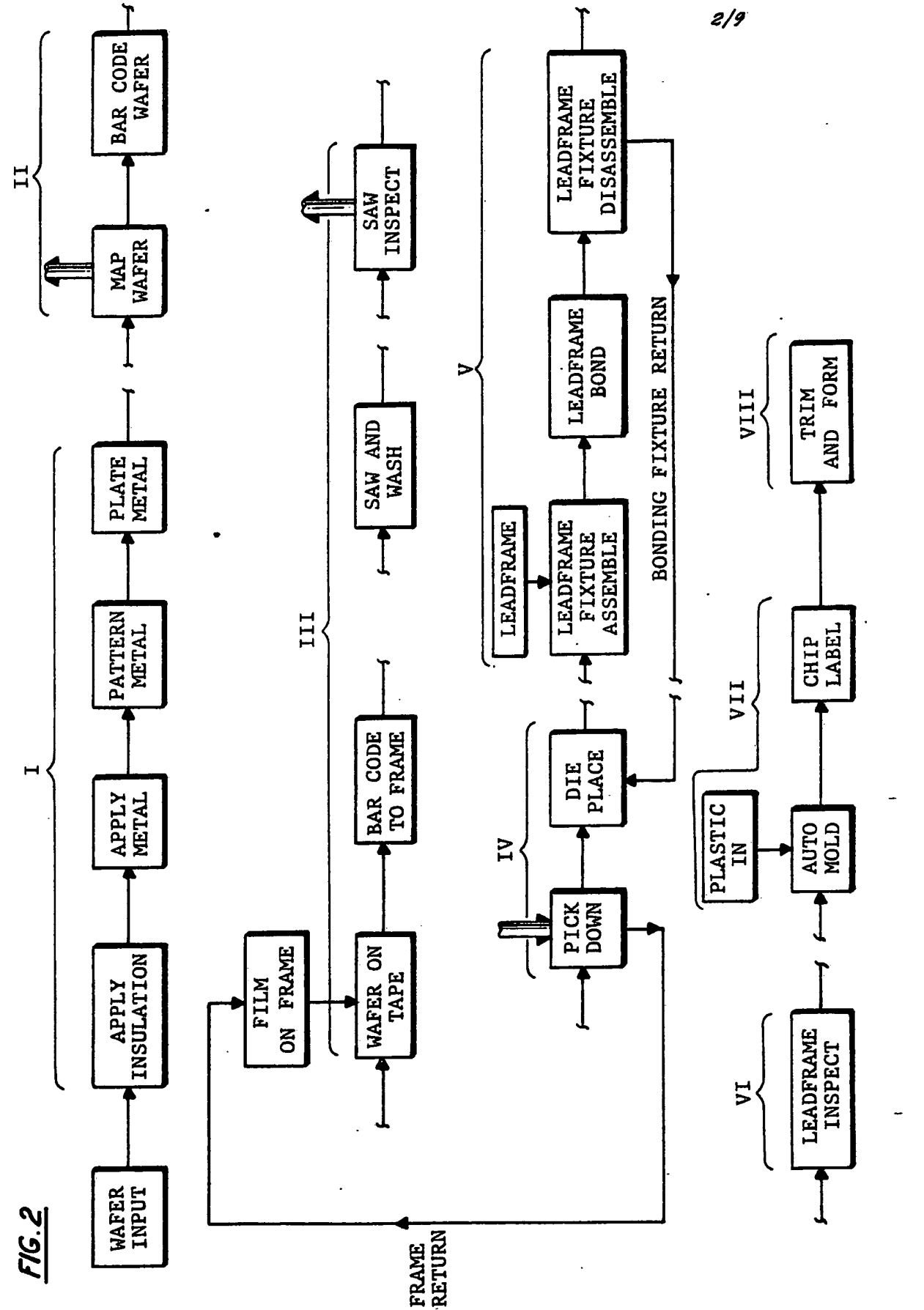

WAFER INPUT
APPLY INSULATION
APPLY METAL
PATTERN METAL
PLATE METAL
MAP WAFER
BAR CODE WAFER
I
II
FILM ON FRAME
WAFER ON TAPE
BAR CODE TO FRAME
SAW AND WASH
SAW INSPECT
III
FRAME RETURN
PICK DOWN
DIE PLACE
IV
LEADFRAME
LEADFRAME FIXTURE ASSEMBLE
LEADFRAME BOND
LEADFRAME FIXTURE DISASSEMBLE
V
BONDING FIXTURE RETURN
PLASTIC IN
AUTO MOLD
CHIP LABEL
VII
TRIM AND FORM
VIII
LEADFRAME INSPECT
VI

FIG.2

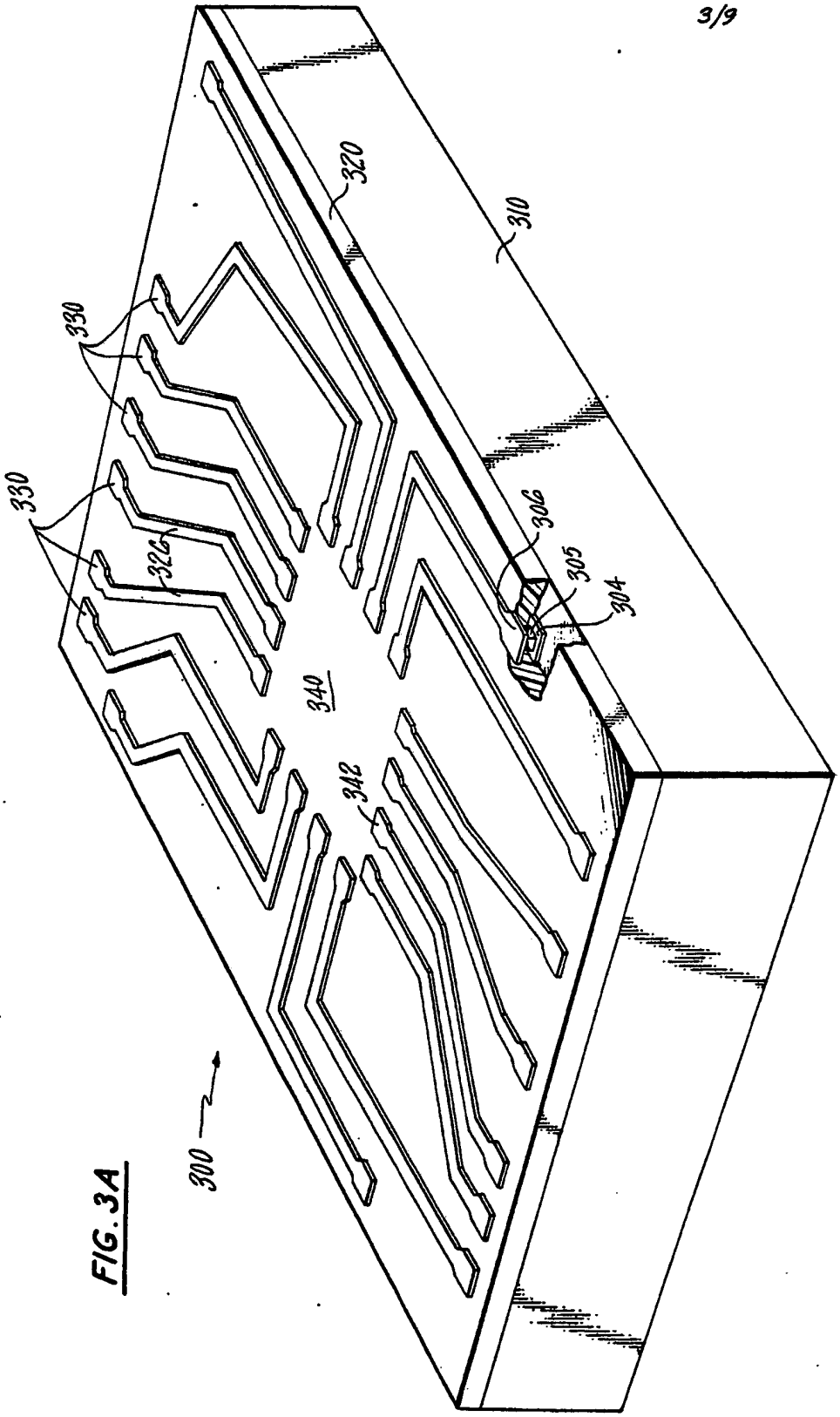


FIG. 3A

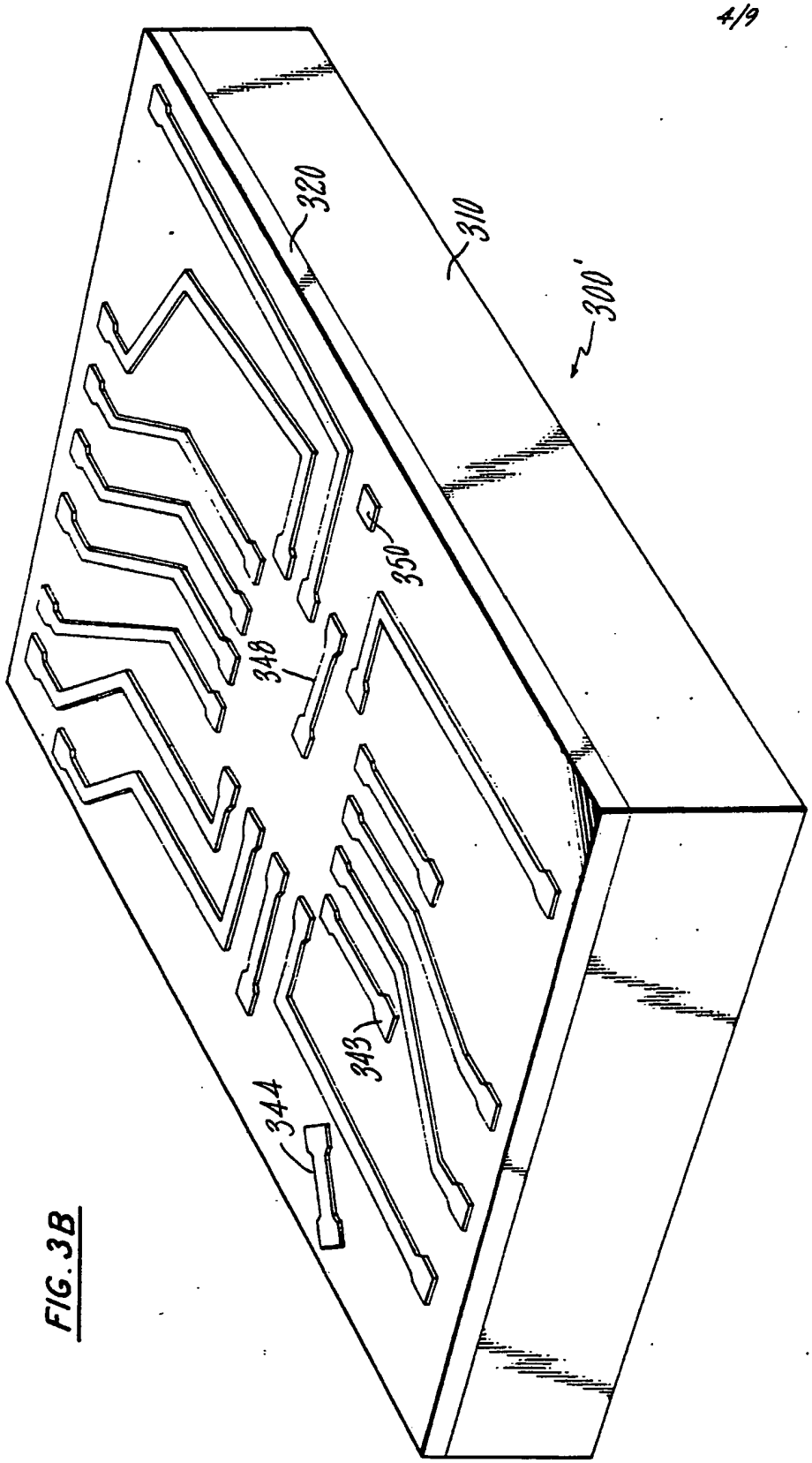


FIG. 3B

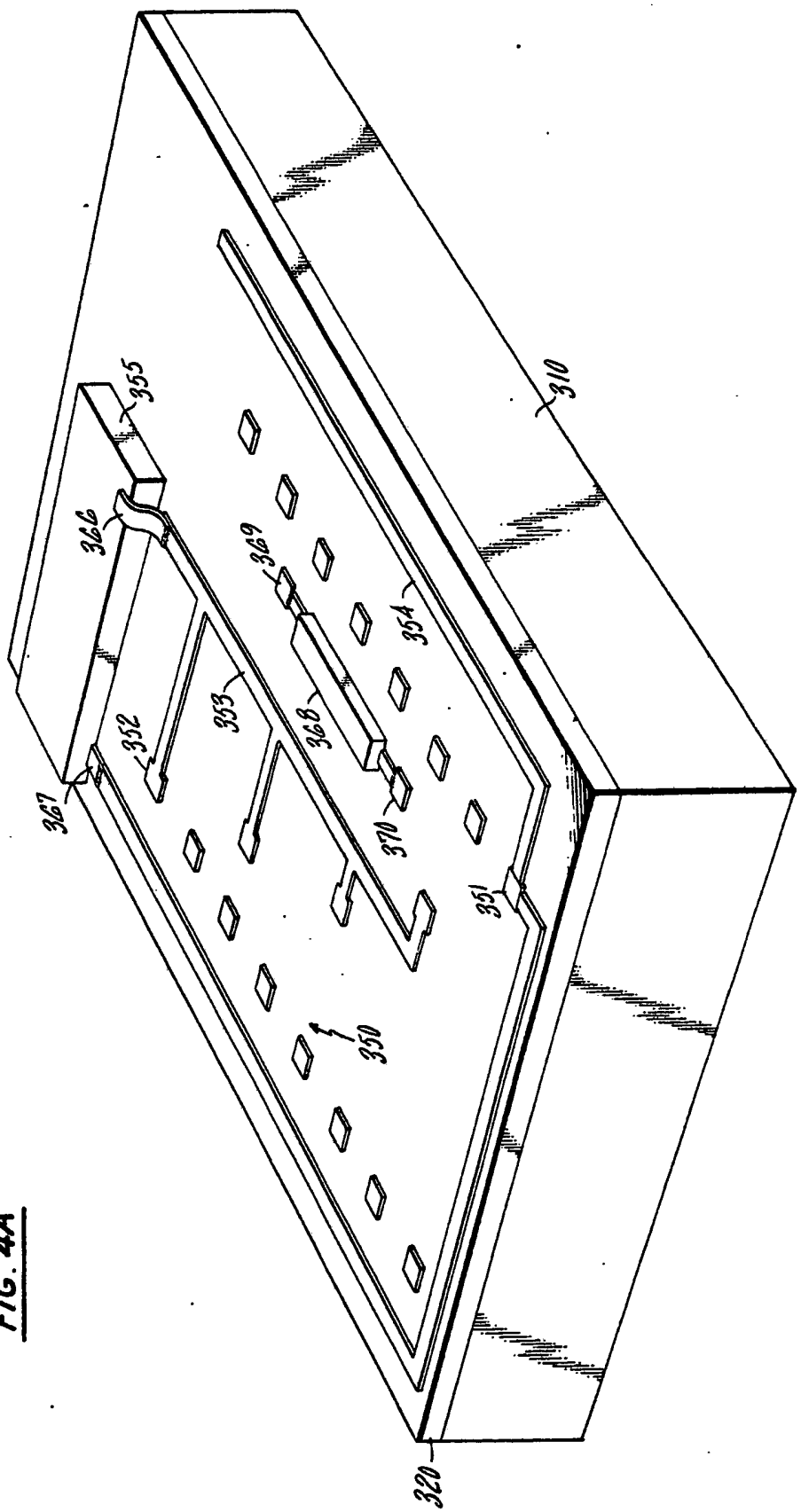


FIG. 4A

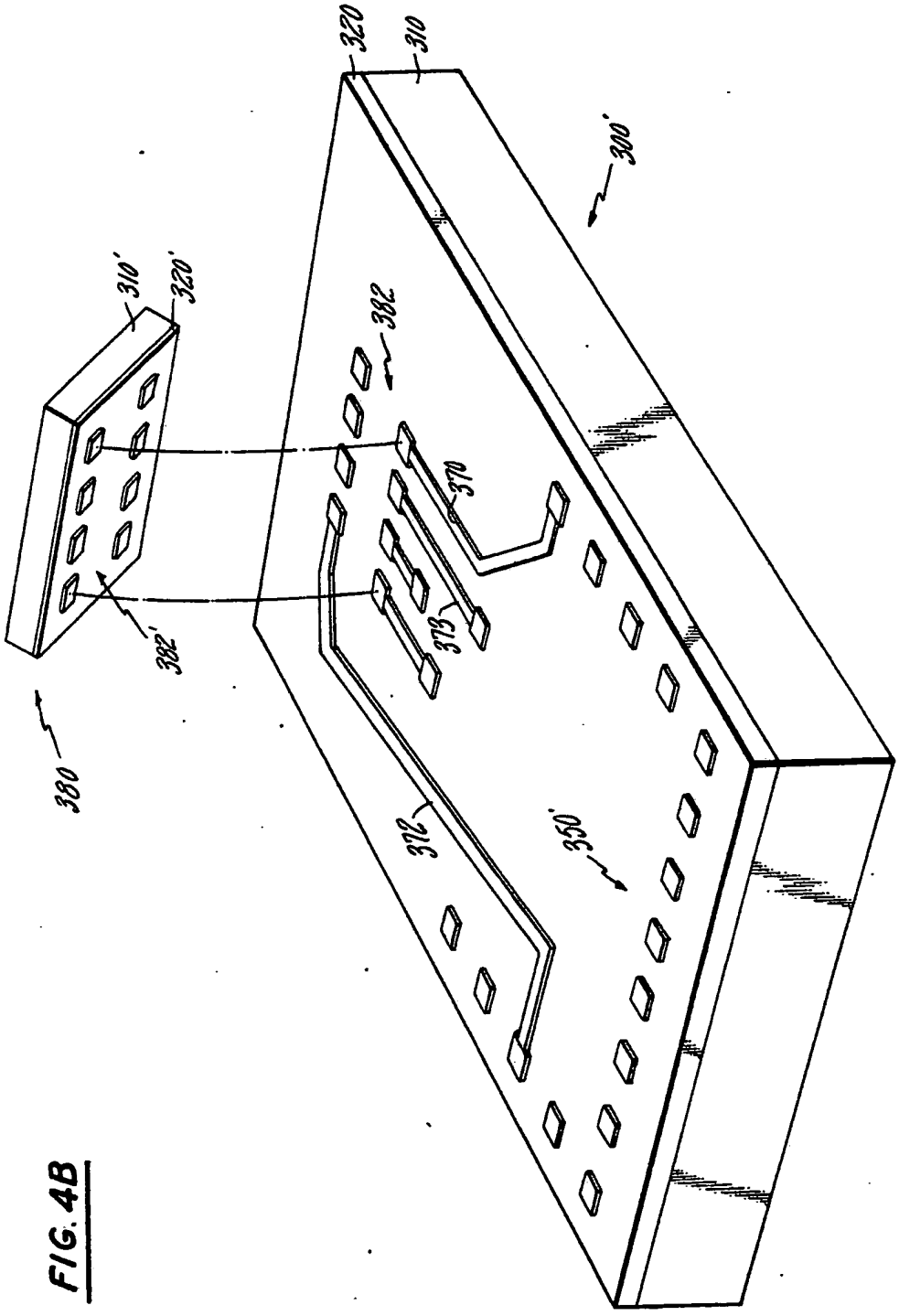


FIG. 4B

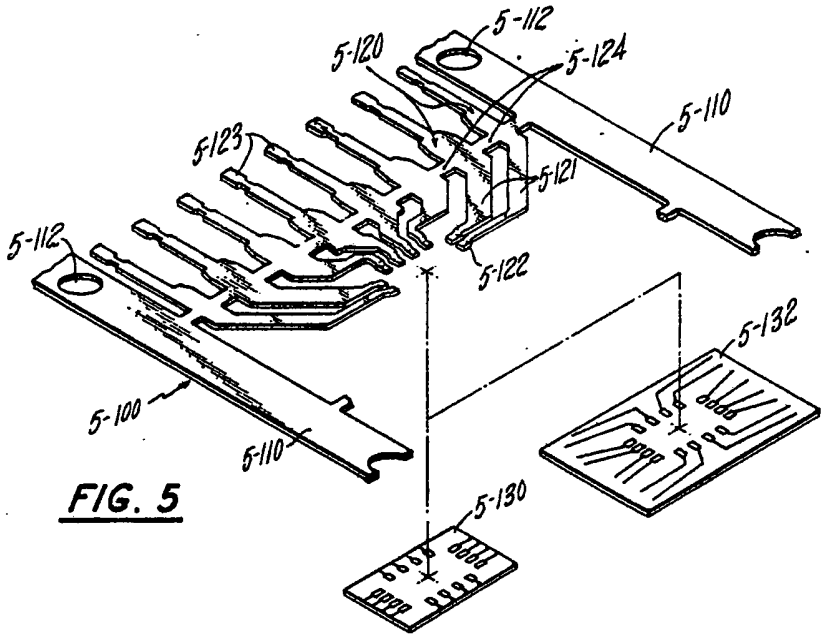


FIG. 5

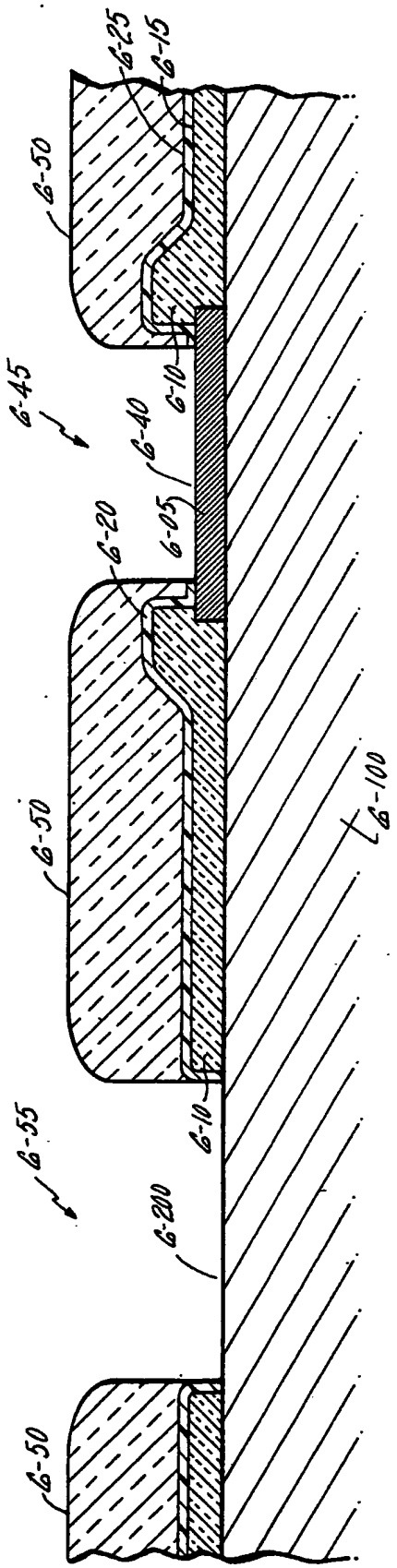
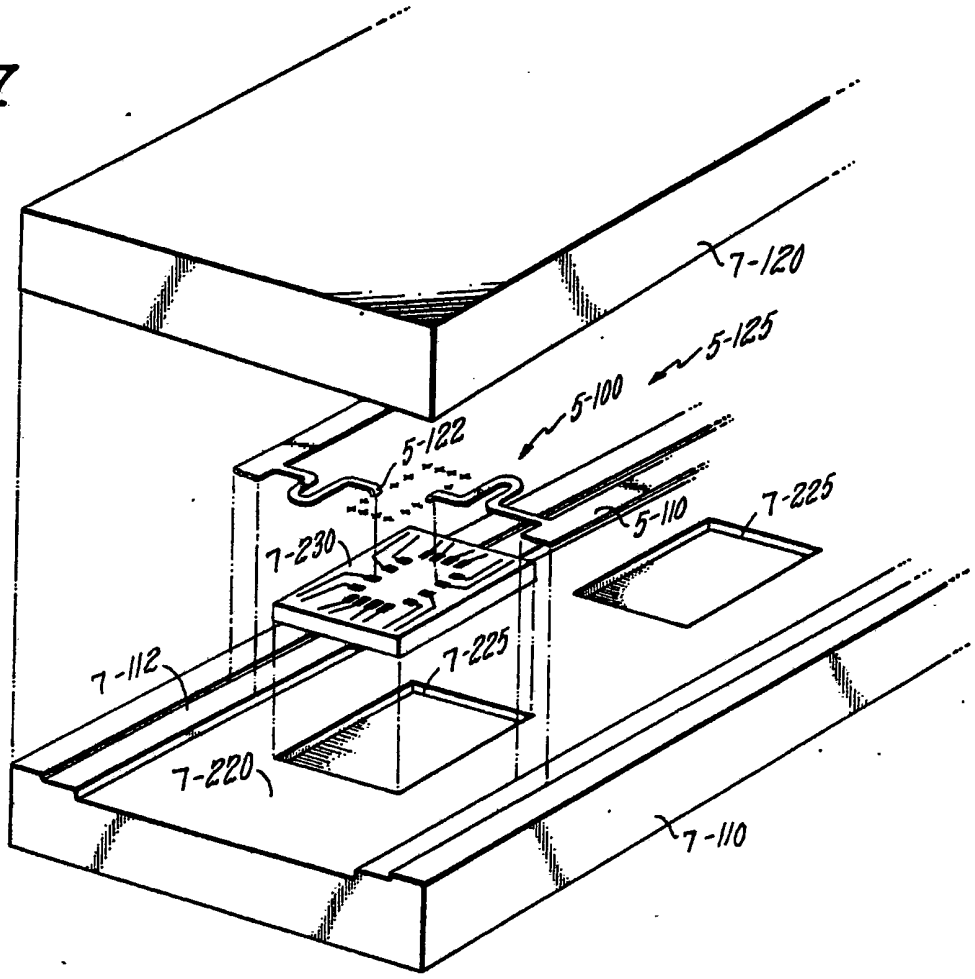


FIG. 6

FIG. 7



INTERNATIONAL SEARCH REPORT

International Application No PCT/US85/00450

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[4] H01L 23/50, 27/04, 27/13, 27/15
U.S. CL. 29/832, 846; 357/17, 40, 41, 51, 68, 71

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	29/832, 846 357/17, 40, 41, 51, 68, 71

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	US, A, 3808475 (BUELOW ET AL) 30 APRIL 1974	1-2
Y	N, Electronics, issued 03 JANUARY 1980, Roger Allan, Thin-film devices on silicon chip can withstand up to 500 C, see pages 39-40	1,3
Y	US, A, 3386008 (LAYER JR. ET AL) 28 MAY 1968	3, 7-12
X	N, IBM Technical Disclosure Bulletin, Vol. 15, No. 2, JULY 1972, Rodendorf et al, Active Silicon Chip Carrier, pages 656-657	1, 3-4,6
Y	US, A, 3947840 (CRAWFORD ET AL) 30 MARCH 1976	1, 4-5
Y	US, A, 3614554 (SHIELD ET AL) 19 OCTOBER 1971	13
A	WO, A, 8201295 (MOTOROLA, INC) 15 APRIL 1982	1-7

* Special categories of cited documents: [15]

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
24 MAY 1985	04 JUN 1985
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	William D. Larkins William D. Larkins

Form PCT/ISA/210 (second sheet) (October 1981)